Electronic Version
Stylesheet Version v1.1.1

[INTEGRATED CIRCUIT MACRO PLACING SYSTEM AND METHOD]

Abstract

A method (300) of placing a to-be-placed integrated circuit macro (404) adjacent one or more already-placed macros (400) aboard an integrated circuit chip (100). The method includes the step of performing a canonical ordering of the edges of the to-be-placed and already placed macros. Then, an edge constraint vector (500, 526) is generated for each active edge (668) of the already-placed macro(s) and each edge of the to-be-placed macro. Each of the edge constraint vectors of the to-be-placed macro is compared to each edge constraint vector of the active edge(s) using a string matching algorithm so as to determine whether any edges of the to-be-placed macro are compatible with any active edges of the already-placed macro(s). The method may be implemented in a CAD system (600).